

## IN THE SPECIFICATION

Please amend the Reference to Related Application at page 2, lines 10-12, as follows:

~~This application is related to and incorporates herein by reference U.S. Application by L. A. Barroso et al., Serial No. \_\_\_\_\_, Attorney Docket No. 18973-53 (P003165), filed \_\_\_\_\_, and entitled "A Scalable Architecture Based on Single chip Multiprocessing."~~

This application is a divisional application of U.S. Patent Application Serial No. 09/877,530, which was filed on June 8, 2001, by L.A. Barroso et al., entitled "Method and System For Exclusive Two-Level Caching in a Chip Multiprocessor." This application is related to and incorporates herein by reference U.S. Patent No. 6,668,308, which issued on December 23, 2003, by L.A. Barroso et al., entitled "A Scalable Architecture Based on Single-Chip Multiprocessing."